Claims

What is claimed is:

1. A transistor memory array comprising:

a first plurality of non-volatile memory transistors and a second plurality of read-only memory transistors, the non-volatile memory transistors having the same footprint as the read-only memory transistors within a single memory array.

2. The memory array of claim 1 wherein said footprint further includes a select transistor.

3. The memory array of claim 2 wherein said footprint has a longitudinal dimension with the select transistor and memory transistor having a common electrode.

4. The memory array of claim 1 wherein the read-only memory transistors include transistors with substrates having open channels and transistors with substrates having shorted channels.

5. The memory array of claim 1 wherein the non-volatile memory transistors have two poly layers and the read-only memory transistors have one poly layer.

6. The memory array of claim 1 wherein the second plurality of read-only memory transistors is grouped into rows.

7. The memory array of claim 6 wherein said group of rows of read only transistors has a first subgroup of transistors in at least one row in a first logic state.

8. The memory array of claim 7 wherein said group of rows of read-only memory transistors has a second subgroup of transistors in at least one row in a second logic state.

9. The memory array of claim 4 wherein the channels in the read-only memory transistors are defined by a buried depletion implant in said substrate, the extent of the implant defining open and shorted channels.

10. The transistor array of claim 1 wherein said non-volatile memory transistors are EEPROM transistors.

11. A method of making a transistor memory array with both read-only memory and rewriteable MOS and CMOS memory transistors, all having subsurface electrodes and channels comprising:

providing a single mask set for forming a memory array of rows and columns of memory transistor sites, at least including masks for forming a subsurface active region, heavily doped first and second, spaced apart depletion implant subsurface regions in the active region defining a channel therebetween, a thin oxide layer, a first polysilicon layer and a second polysilicon layer spaced apart from and over the first polysilicon layer;

for a first set of memory transistor sites, blocking mask portions for forming the second depletion implant subsurface region to the extent that the channel is extended to impede transistor conductivity, the mask set further modified by blocking formation of the thin oxide layer and the first polysilicon layer, thereby forming read-only memory transistor cells that are open at the first set of sites;

for a second set of memory transistor sites, increasing the first and second depletion implant subsurface regions to the extent that the channel is shorted to establish permanent transistor conductivity at the second set of sites, the mask set further modified by blocking formation of the thin oxide layer and the first polysilicon layer; and

for a third set of memory transistor sites, using the single mask set to form EEPROM memory transistor cells.

12. The method of claim 11 further defined by grouping the first and second sets of memory transistor sites in a first group of rows and grouping the EEPROM memory transistors in a second group of rows.

13. The method of claim 11 further defined by establishing an active region using the single mask set and forming a select transistor adjacent to the memory transistor.

14. The method of claim 13 further defined by forming the active region as a longitudinal region with opposed edges, the active region having buried n subsurface regions for at least the memory transistors.

15. A method of making a transistor memory array comprising:

establishing an array with rows and columns of memory cells, each cell having an active area of a specified longitudinal dimension sufficient in length for formation of both a non-volatile memory cell and a read-only memory cell.

16. The method of claim 15 wherein the memory array comprises rows and columns of transistor cells with a first plurality of rows of non-volatile memory cells and a second plurality of read-only memory transistor cells.

17. The method of claim 15 further defined by forming a select transistor within the active area for both non-volatile memory transistor cells and read-only memory transistor cells.

18. The method of claim 15 further defined by providing two poly layers for the plurality of non-volatile memory transistor cells and a single poly layer for the read-only memory transistor cells.

19. The method of claim 16 further defined by programming the read-only memory transistor cells at the time of manufacture with pre-defined data consisting of ones and zeros.